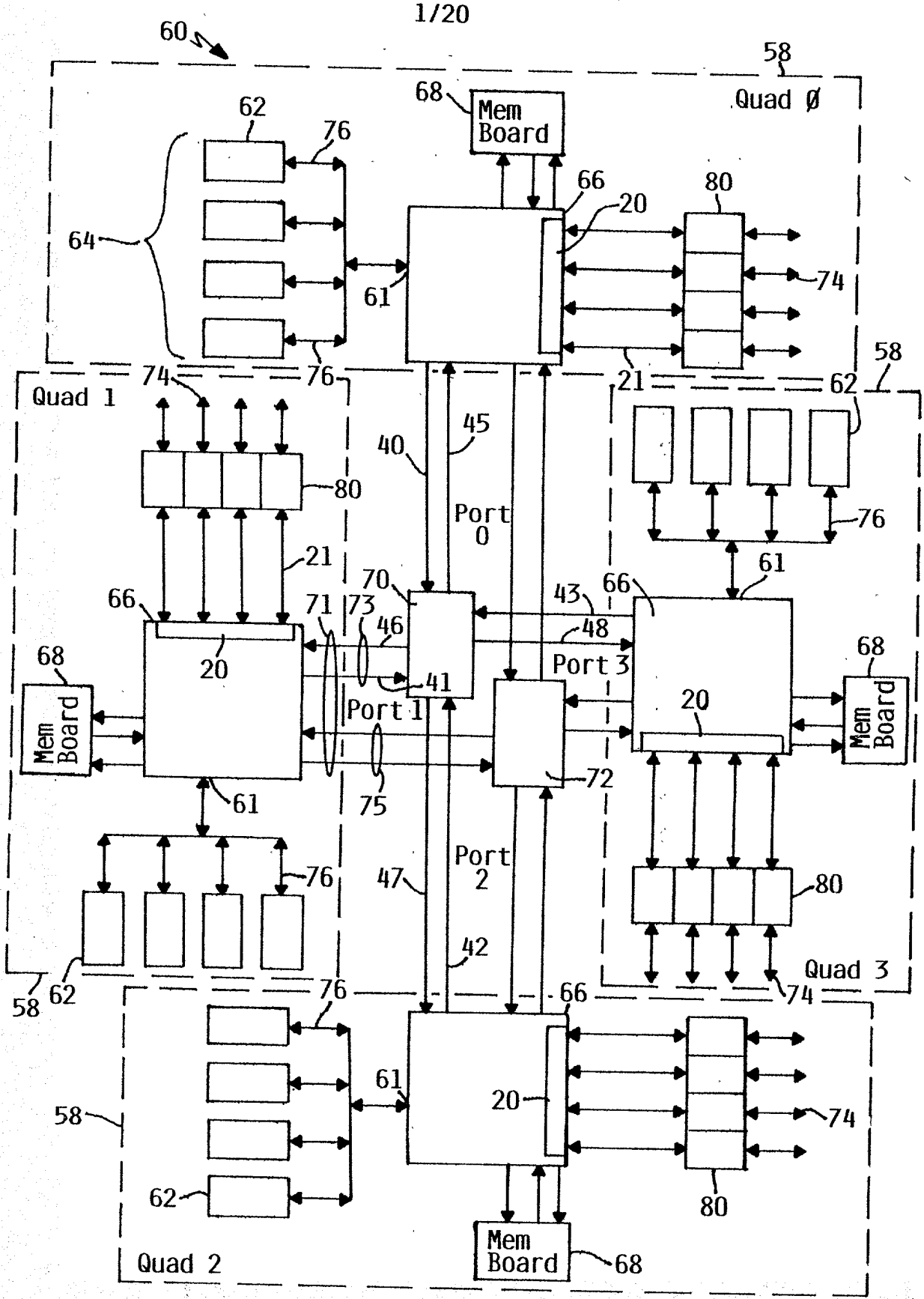
60
58
Quad Ø
Quad 1
Quad 2
Quad 3
Mem Board
Port 0
Port 1
Port 2
Port 3
62
64
76
68
66
20
80
74
61
21
40
45
70
71
73
46
48
43
41
72
75
47
42

FIG. 1

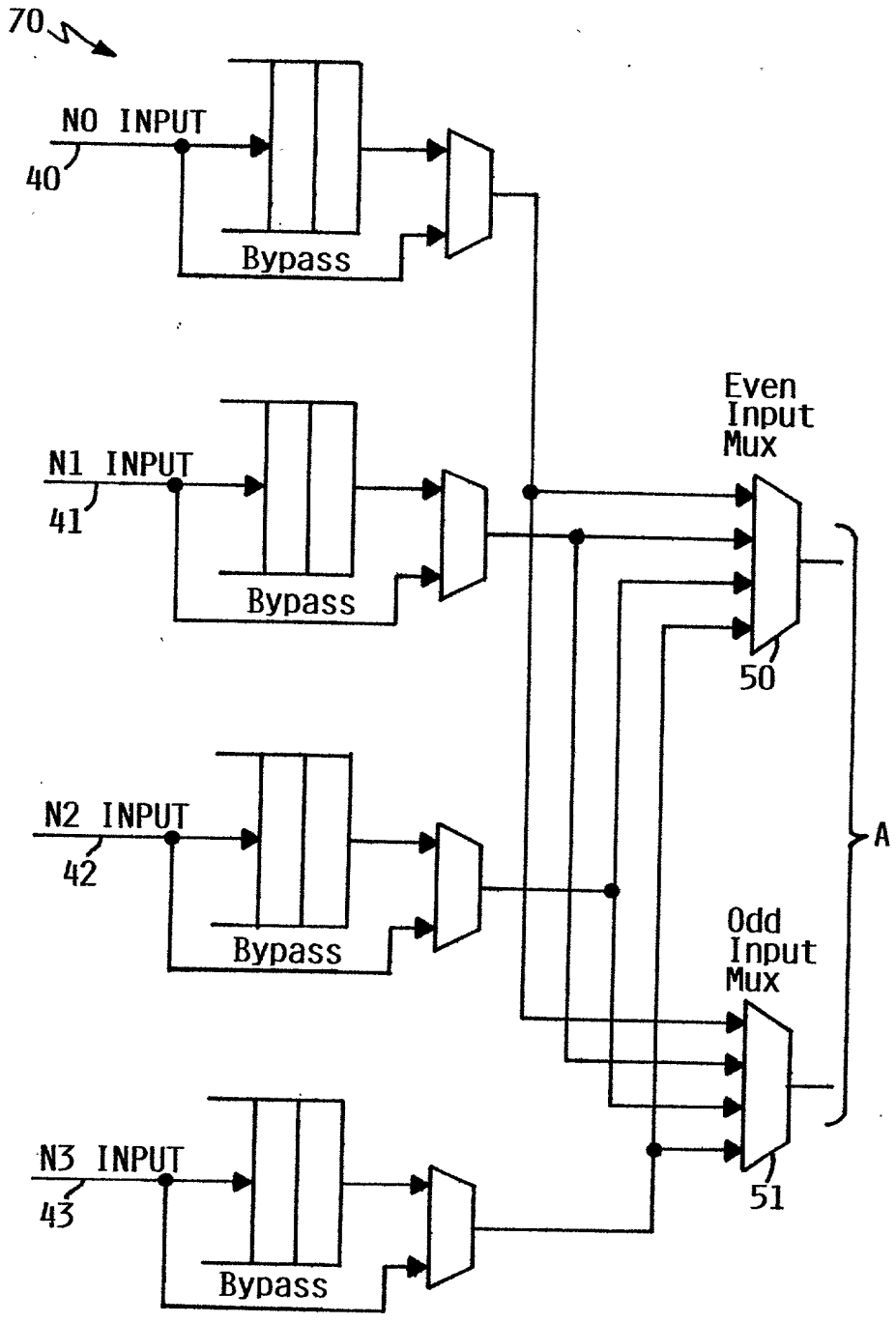
70
NO INPUT
40
Bypass
N1 INPUT
41
Bypass
N2 INPUT
42
Bypass
N3 INPUT
43
Bypass
Even Input Mux
50
Odd Input Mux
51
A

FIG. 2A

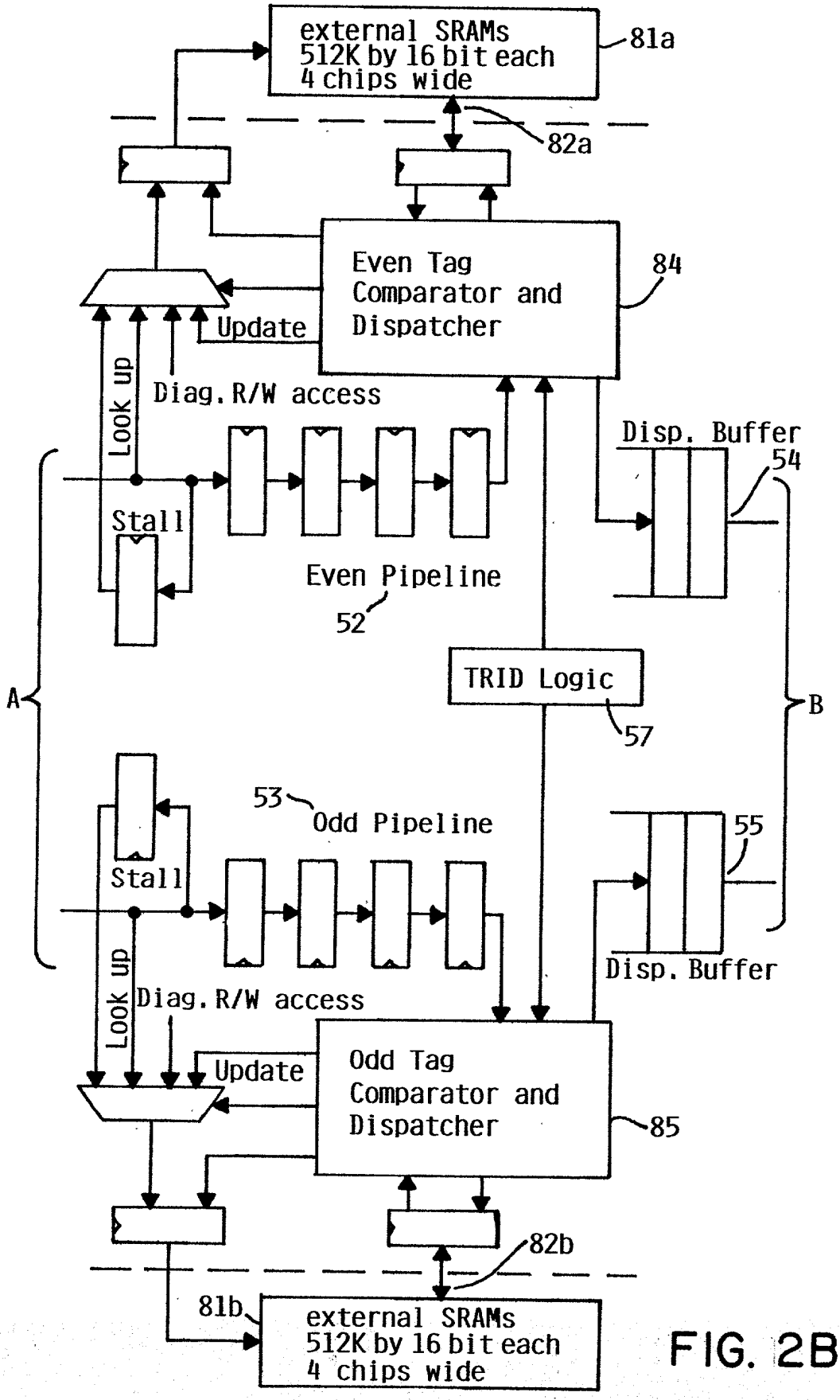
external SRAMs
512K by 16 bit each
4 chips wide
81a
82a
Even Tag
Comparator and
Dispatcher
84
Update
Look up
Diag. R/W access
Disp. Buffer
54
Stall
Even Pipeline
52
TRID Logic
57
A
B
53
Odd Pipeline
55
Stall
Disp. Buffer
Look up
Diag. R/W access
Update
Odd Tag
Comparator and
Dispatcher
85
82b
81b
external SRAMs
512K by 16 bit each
4 chips wide

FIG. 2B

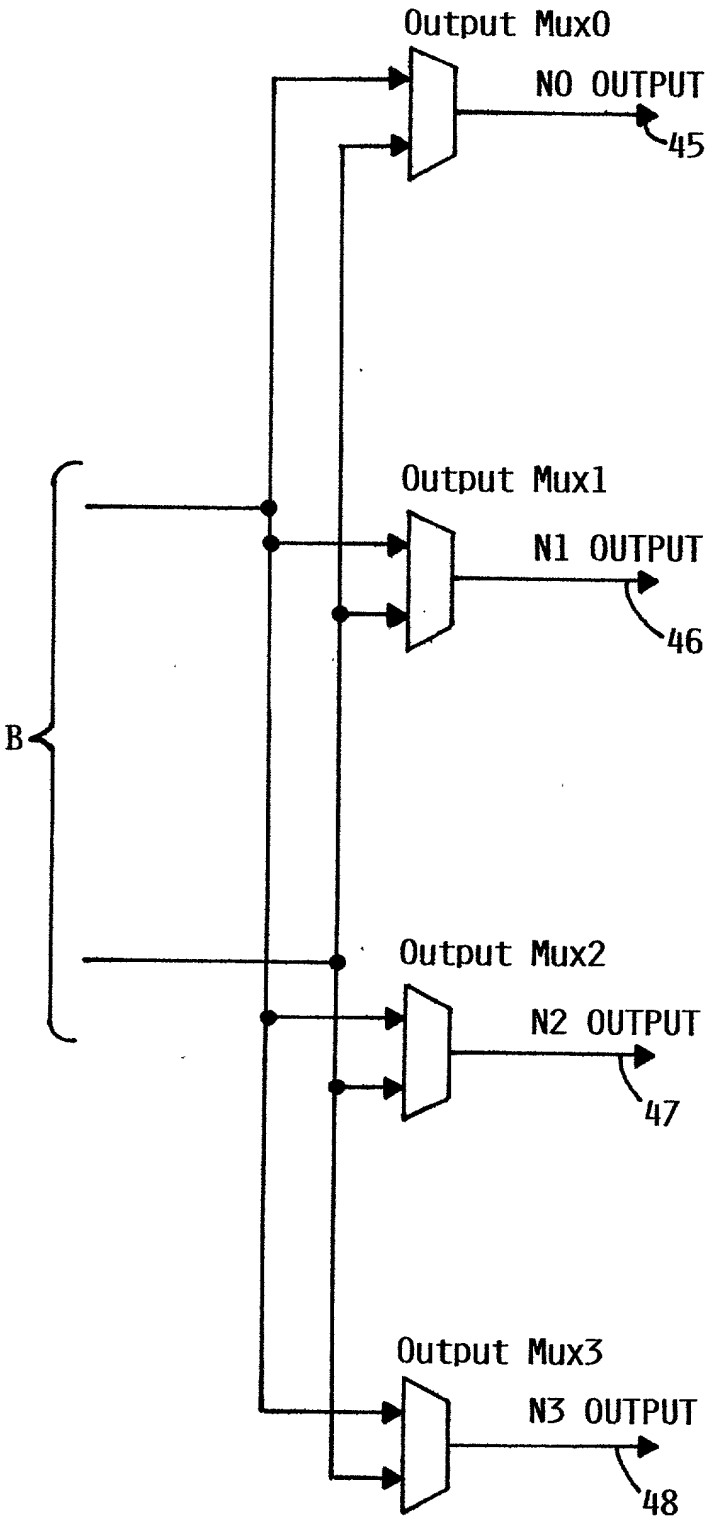
Output Mux0
NO OUTPUT
45
Output Mux1
N1 OUTPUT
46
B
Output Mux2
N2 OUTPUT
47
Output Mux3
N3 OUTPUT
48

FIG. 2C

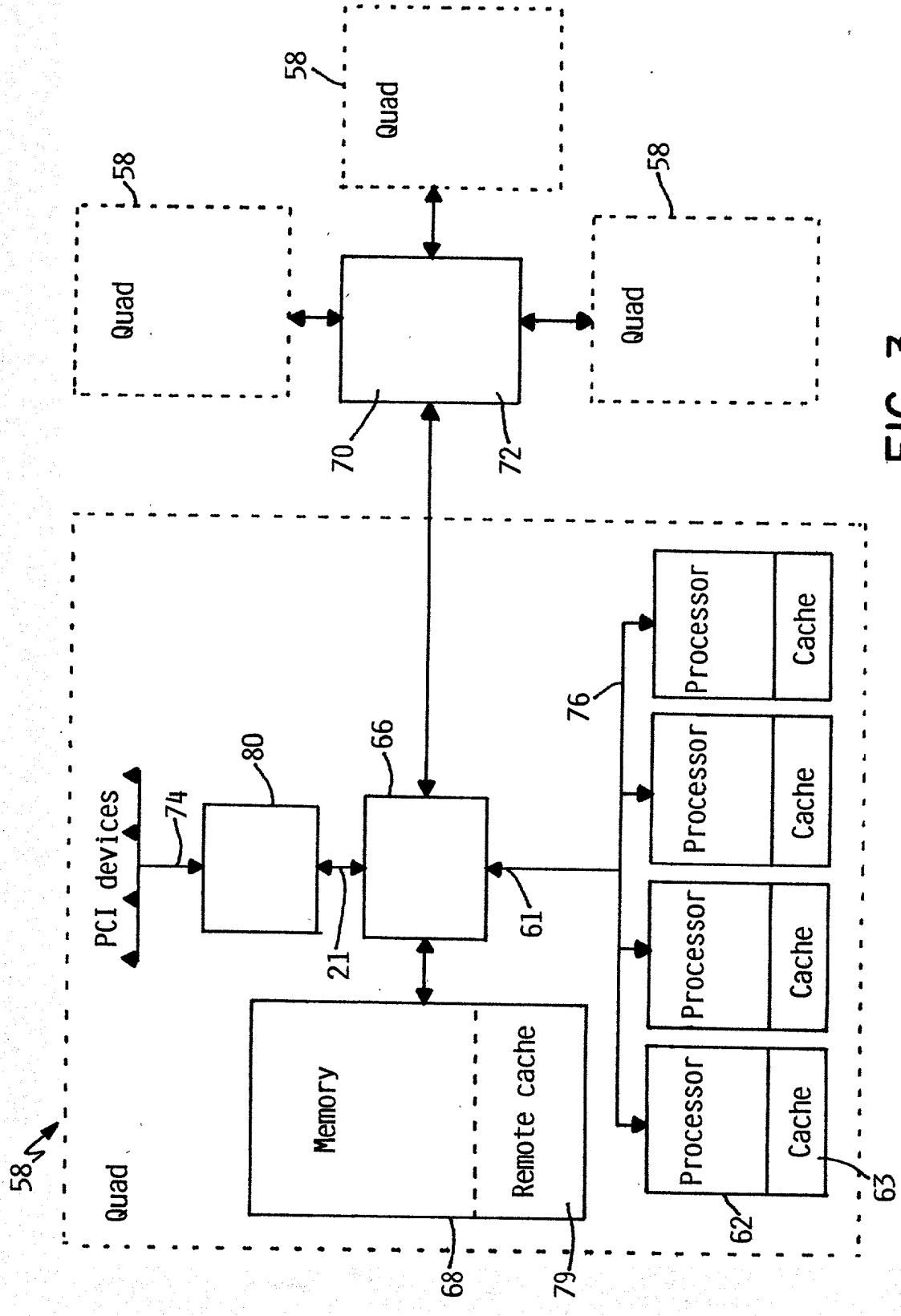
58
Quad
58
Quad
58
Quad
70
72
58
Quad
PCI devices
74
80
66
21
61
76
Memory
Remote cache
68
79
Processor
Cache
Processor
Cache
Processor
Cache
Processor
Cache
62
63

FIG. 3

101 Bus 73 Request	102 Global RC State	103 Xbar 70 Resp to Req	104 Xbar 70 Req to Home	105 Xbar 70 Req to Sharers
LCR	Invalid	GO Excl	-	-
	Shared Miss	GO	-	-
	Dirty Miss	WAIT	-	-
	Mod Miss	WAIT Excl	-	-
	Invalid	WAIT	LCR	-
	Shared Miss	WAIT	LCR	-
	Shared Hit	GO	-	-
	Shared Both	GO	-	-
RCR	Dirty Miss	WAIT	-	-
	Dirty Hit	GO	-	-
	Dirty Both	GO	-	-
	Dirty Mod	GO	-	-
	Mod Miss	WAIT	-	-
	Mod Hit	GO Excl	-	-

A

B

FIG. 4A

106 Xbar 70 Req to Owner	107 Next Global RC State	108 RC Allocate and/or Rollout	Comments
-	n/c	NO	Line is Home
-	n/c	NO	Clean shared
RCR	Shared Miss	NO	Wash dirty to clean
RCRI	Invalid	NO	Line owned by another send the line Home
-	Shared Hit	YES	Home to shared
-	Shared Both	YES	Add req to sharing list
-	n/c	NO	Read hit
-	n/c	NO	Read hit
RCR	Dirty Both	YES	Add req to sharing list
-	n/c	NO	Read hit
-	n/c	NO	Read hit
-	n/c	NO	Read hit
RCR	Dirty Hit	YES	Add req to sharing list
-	n/c	NO	Allow L2 cache to be E state

A

C

FIG. 4B

B

LCRI (109)	Invalid	GO	-	-
	Shared Miss	GO inv=n	-	n*RCI
	Dirty Miss	WAIT inv=n	-	n*RCI
	Mod Miss	WAIT	-	-
RCRI	Invalid	WAIT	LCRI	-
	Shared Miss	WAIT inv=n	LCRI	n*RCI
	Shared Hit	GO inv=1	LCI	-
	Shared Both	GO inv=n+1	LCI	n*RCI
	Dirty Miss	WAIT inv=n	-	n*RCI
	Dirty Hit	GO inv=1	-	-
	Dirty Both	GO inv=n+1	-	n*RCI
	Dirty Mod	GO inv=n	-	n*RCI
	Mod Miss	WAIT	-	-
	Mod Hit	GO	-	-

D

FIG. 4C

C

D

-	n/c	NO	Already home
-	Invalid	NO	Shared to home
RCRI	Invalid	NO	Send the line home
RCRI	Invalid	NO	Send the line home
-	Mod Hit	YES	Line was home
-	Mod Hit	YES	Line was shared
-	Mod Hit	NO	Line was shared
-	Mod Hit	NO	Line was shared
RCRI	Mod Hit	YES	Line was dirty, owner replies
RCI	Mod Hit	NO	Use own shared copy
RCI	Mod Hit	NO	Use own shared copy
-	Mod Hit	NO	Use own modified copy
RCRI	Mod Hit	YES	Owner returns line
-	n/c	NO	Already modified exclusively

FIG. 4D

Bus 73 Request	Global RC State	Xbar 70 Resp to Req	Xbar 70 Req to Home	Xbar 70 Req to Sharers
LUR	Invalid	GO	-	-
	Shared Miss	GO	-	-
	Dirty Miss	Wait	-	-
	Mod Miss	Wait	-	-
RUR	Invalid	Wait	LUR	-
	Shared Miss	Wait	LUR	-
	Shared Hit	GO	-	-
	Shared Both	GO	-	-
	Dirty Miss	WAIT	-	-
	Dirty Hit	GO	-	-
	Dirty Both	GO	-	-
	Dirty Mod	GO	-	-
	Mod Miss	WAIT	-	-
	Mod Hit	GO	-	-

A

FIG. 5A

A

Xbar 70 Req to Owner	Next Global RC State	RC Allocate and/or Rollout	Comments
-	n/c	NO	
-	n/c	NO	
RUR	n/c	NO	
RUR	n/c	NO	
-	n/c	NO	
-	n/c	NO	
-	n/c	NO	
-	n/c	NO	
-	n/c	NO	
RUR	n/c	NO	
-	n/c	NO	
-	n/c	NO	
-	n/c	NO	
RUR	n/c	NO	
-	n/c	NO	

FIG. 5B

Bus 73 Request	Global RC State	Xbar 70 Resp to Req	Xbar 70 Req to Home	Xbar 70 Req to Sharers	Xbar 70 Req to Owner	Next Global RC State	RC Allocate and/or Rollout	Comments
LUW (partial)	Invalid	GO	-	-	-	n/c	NO	
	Shared Miss	GO inv=n	-	n*RCI	-	Invalid	NO	
	Dirty Miss	WAIT inv=n	-	n*RCI	RCRI	Invalid	NO	
	Mod Miss	WAIT	-	-	RCRI	Invalid	NO	
RUW (partial)	Invalid	WDAT	LRMW	-	-	n/c	NO	Get it from Home, then send it back
	Shared Miss	WDAT inv=n	LRMW	n*RCI	-	Invalid	NO	Get it from Home, then send it back
	Shared Hit	GO inv=1	LCI	-	-	Mod Hit	NO	Upgrade from Shared to Mod
	Shared Both	GO inv=n+1	LCI	n*RCI	-	Mod Hit	NO	Upgrade from Shared to Mod
	Dirty Miss	WDAT inv=n	LWB	n*RCI	RCRI	Invalid	NO	Get it from Owner, then send it Home
	Dirty Hit	GO inv=1	-	-	RCI	Mod Hit	NO	Upgrade from Dirty to Mod
	Dirty Both	GO inv=n+1	-	n*RCI	RCI	Mod Hit	NO	Upgrade from Dirty to Mod
	Dirty Mod	GO inv=n	-	n*RCI	-	Mod Hit	NO	Upgrade from Dirty to Mod
	Mod Miss	WDAT	LWB	-	RCRI	Invalid	NO	Get it from Owner, then send it Home

A

FIG. 6A

FIG. 6B

A

	Mod Hit	GO	-	-	-	n/c	NO	Ready as is
LUW (full line)	Invalid	GO	-	-	-	n/c	NO	Already Home
	Shared Miss	GO inv=n	-	n*RCI	-	Invalid	NO	Invalidate Sharers
	Dirty Miss	GOnP7 inv=n+1	-	n*RCI	RCI	Invalid	NO	Invalidate Mod line at Owner and Sharers
	Mod Miss	GOnP7 inv=1	-	-	RCI	Invalid	NO	Invalidate Mod line at Owner
RUW (full line)	Invalid	WTGT inv=1	LUW	-	-	n/c	NO	Write to Home
	Shared Miss	WTGT inv=n+1	LUW	n*RCI	-	Invalid	NO	Invalidate owner and write to Home
	Shared Hit	GO inv=1	LCI	-	-	Mod Hit	NO	Invalidate Home and upgrade your S to M
	Shared Both	GO inv=n+1	LCI	n*RCI	-	Mod Hit	NO	Invalidate Home and other RC's upgrade your S to M
	Dirty Miss	WTGT inv=n+1	LWB	n*RCI	RCI	Invalid	NO	Invalidate all RC's and write to Home
	Dirty Hit	GO inv=1	-	-	RCI	Mod Hit	NO	Invalidate owner's RC and upgrade your S to M
	Dirty Both	GO inv=n+1	-	n*RCI	RCI	Mod Hit	NO	Invalidate all other RC's and upgrade your S to M
	Dirty Mod	GO inv=n	-	n*RCI	-	Mod Hit	NO	Invalidate other RC's and update own RC
	Mod Miss	WTGT inv=1	LWB	-	RCI	Invalid	NO	Invalidate owner and write to Home
	Mod Hit	GO	-	-	-	n/c	NO	Update own RC

Bus 73 Request	Xbar 70 Resp to Req	Xbar 70 Req to Target	Xbar 70 Req to Others	Comments
MMR	WAIT	MMR	-	Remote MMIO or CSR
MMW	WTGT inv=1	MMW	-	Remote MMIO or CSR
INTR	WTGT inv=1	INTR	-	Remote interrupt
TLBP	TLBR inv=all-1	TLBP	TLBP	Purge TLB to all in partition
SYNC bit has been set	-	SYNC w/o ttrid	SYNC w/o ttrid	SYNC to all in partition clear SYNC bit
any request with abort	-	-	-	Any request that is aborted will be ignored

FIG. 7

Bus 73 Request	Global RC State of Y	Xbar 70 Req to Home	Xbar 70 Req to Instig.	Xbar 70 Req to Sharers
request of line X instigates RC rollout of line Y	Shared Hit	CI	RCI	-
	Shared Both	CI	RCI	-
	Dirty Hit	-	RCI	-
	Dirty Both	-	RCI	-
	Dirty Mod (>1 sharer)	-	RCI	CI to new owner
	Dirty Mod (1 sharer)	-	RCI	CI to new owner
	Mod Hit	LWB	RCRI	-

A

FIG. 8A

A

Xbar 70 Req to Owner	Next Global RC State of Y	Comments
-	Invalid	Invalidate only read copy.
-	Shared Miss	Another read copy still exists.
CI	Mod Miss	Invalidate only read copy of dirty line-only owner still exists.
CI	Dirty Miss	Requester's shared copy is invalidated, line remains dirty.
-	Dirty Miss	Another sharer exists after upgrading a sharer to an owner-choose new owner.
-	Mod Miss	Upgrade only sharer to be new owner.
-	Invalid	Only copy is modified - line is written home.

FIG. 8B

Mnemonic	Code	Description	Q/A
LUR	00100	request for a local uncached read (either partial or full)	Q
LUW	00101	request for a local uncached write (either partial or full)	Q
GO	00110	reply to Control agent 66 that validates speculative access with bus 76	A
GOnP7	00111	reply to Control agent 66 that validates speculative access without bus 76	A
LCR	01000	request for a cached read to a local address	Q
LRMW	01001	request to Control agent 66 for a cached read-modify-write	Q
WAIT	01011	reply to Control agent 66 canceling speculative access, Data Crossbar 72 completion	A
LCRI	01100	request for a cached read-invalidate to a local address	Q
LCI	01100	LCRI request where all BE are zero, an invalidate	Q

A

FIG. 9A

A

LWB	01101	request to Control agent 66 for full local line cached writeback	Q
ERR	01111	reply to Control agent 66 that cancels the request and posts an error	A
SYNC	10000	request to Control agent 66 that synchronizes the microsecond clock	Q
RTRY	10001	reply to Control agent 66 that cancels the request, it must be retried	A
WDAT	10010	reply to Control agent 66 for a partial write request, returns target info	A
WTGT	10011	reply to Control agent 66 for a full line write request, returns target info	A
RUR	10100	request for a remote uncached read (either partial or full line)	Q
RUW	10101	request to crossbar 70 for remote uncached write (partial or full)	Q
MMR	10110	request for a memory-mapped read	Q

B

FIG. 9B

B

MMW	10111	request for a memory-mapped write	Q
RCR	11000	request for a cached read to a remote address	Q
CI	11010	request to Control agent 66 to collect invalidate acknowledges	Q
INTR	11011	request to forward an interrupt to the target quad	Q
RCRI	11100	request for a cached read-invalidate to a remote address	Q
RCI	11100	RCRI request where all BE are zero, an invalidate	Q
TLBP	11101	request for a TLB purge, only one active at a time	Q
TLBR	11110	reply to a prior TLBP request, only one active at a time	A
ABRT	11111	request started by Control agent 66 is aborted, ignore 1st half-transfer	Q

FIG. 9C

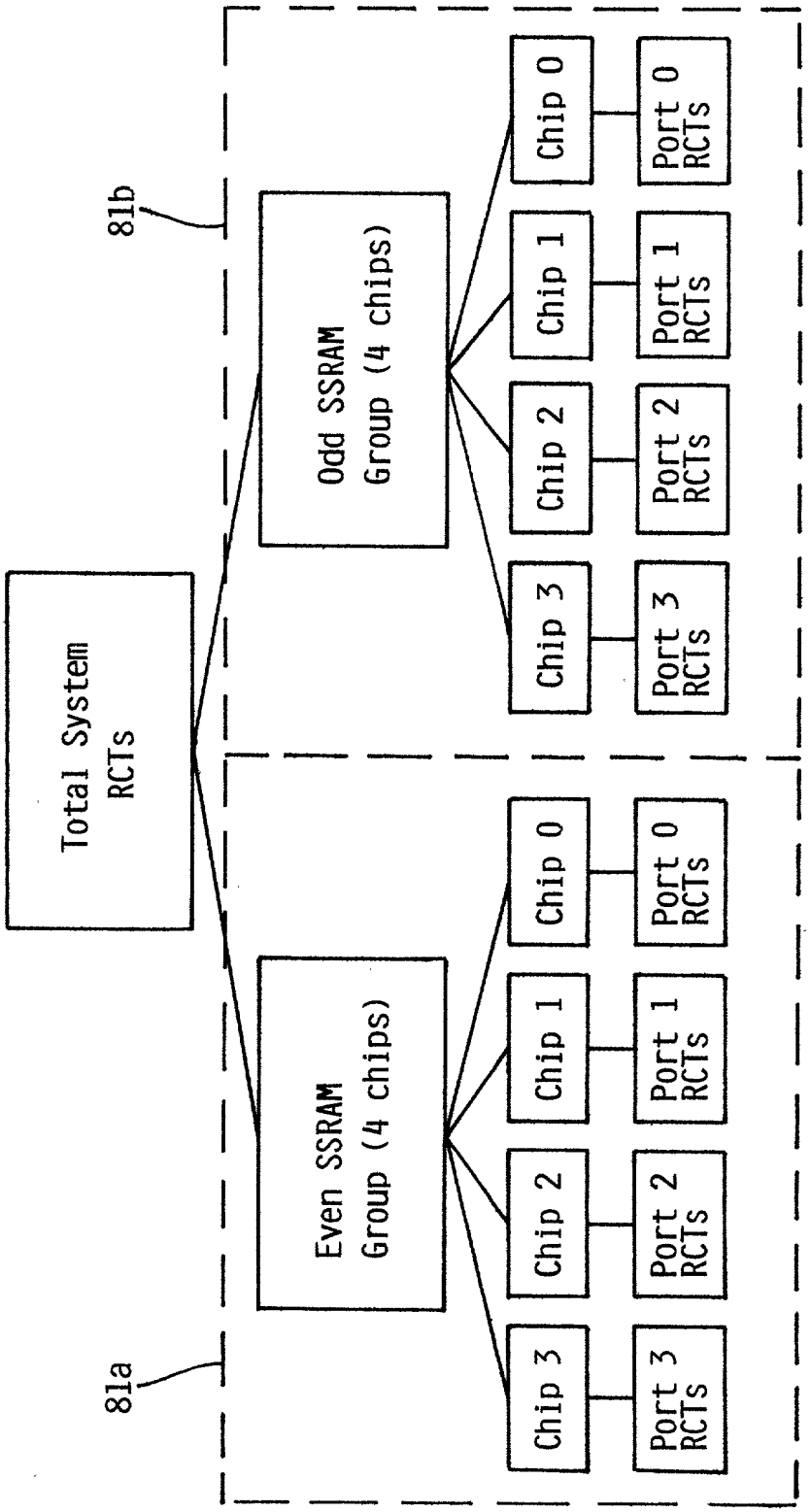
Total System RCTs
81a
81b
Even SSRAM Group (4 chips)
Odd SSRAM Group (4 chips)
Chip 0
Chip 1
Chip 2
Chip 3
Port 0 RCTs
Port 1 RCTs
Port 2 RCTs
Port 3 RCTs

FIG. 10